## Chip Multilayer Ceramic Capacitors for Implantable Medical Devices (Non Life support circuit)

### GCH21A5C2J100FX01\_(0805, C0G:EIA, 10pF, DC630V)

\_: packaging code

## **Reference Sheet**

#### 1.Scope

This product specification is applied to Chip Multilayer Ceramic Capacitors used for Implantable Medical Devices (Non Life support circuit).

### 2.MURATA Part NO. System



### 3. Type & Dimensions



				(Unit:mm)
(1)-1 L	(1)-2 W	(2) T	e	g
2.0±0.2	1.25±0.2	1.0+0/-0.3	0.3 min.	0.7 min.

#### 4.Rated value

(3) Temperature (Public STD C	(4) Rated	(5) Nominal	(6) Conscitones	Specifications and Test Methods			
Temp. coeff or Cap. Change	Temp. Range (Ref.Temp.)	Voltage	Capacitance	Tolerance	(Operating Temp. Range)		
0±30 ppm/°C	25 to 125 °C (25 °C)	DC 630 V	10 pF	±1 %	-55 to 125 °C		

 Soldering Method Flow / Reflow

#### 5.Package

mark	(8) Packaging	Packaging Unit
D	∮180mm Reel PAPER W8P4	4000 pcs./Reel
J ¢330mm Reel PAPER W8P4		10000 pcs./Reel

Product specifications in this catalog are as of May.29,2020,and are subject to change or obsolescence without notice. Please consult the approval sheet before ordering.

Please read rating and !Cautions first.

## Specification and Test Methods

No.	lo. Test Item		Specification				Test Method	ł	
1	Pre-and Post-Stress Electrical Test			_	-				
2	Temperature Cycling		The measured and observed characteristics should satisfy the specifications in the following table.	Fix un	Fix the capacitor to the supporting jig in the same manner and under the same conditions as (12). Perform the 100 cycles			nanner and D cycles	
		Appearance	No marking defects	ac	according to the four neat treatments listed in the following ta				
		Capacitance Change	Within ±2.0% or ±0.3pF	Le	t sit for 24±	2h at room	condition*, the	en measure.	
			(Whichever is larger)	$-\Gamma$	Step	1	2	3	4
		Q	Q ≥ 1,000	┛┝		-55+0/-3	Room Tomp	125+3/-0	Room Tomp
		I.R.	More than 10,000M $\Omega$ or 100 M $\Omega$ · $\mu$ F		Temp.( C)	-00+0/-0	Room remp.	120+0/-0	Room remp.
			(Whichever is smaller)	ľĽ	Time(min.)	15±3	1	15±3	1
3	Destru	uctive Phisical Analysis	No defects or abnormalities	Pe	er EIA-469				
4	Biase	d Humidity	The measured and observed characteristics should satisfy the specifications in the following table.	Ap at	oply the rate 85±3°C and	ed voltage and 80% to 85	nd DC1.3+0.2 % humidity fo	?/-0 V (add 6 or 240±12h.	.8kΩ resistor)
	i í	Appearance	No marking defects	Re	emove and	let sit for 24	±2h at room o	condition*, th	en measure.
	i í	Capacitance Change	Within ±3.0% or ±0.3pF	the	en measure	).			
	1		(Whichever is larger)	The	The charge/discharge current is less than 50mA.				
	i I	Q	Q ≥ 200						
	i I	I.R.	More than 1,000M $\Omega$ or 50 M $\Omega$ · $\mu$ F						
			(Whichever is smaller)						
5	Operational Life		The measured and observed characteristics should	Apply 120% of the rated voltage for 1,000±12h at 125±3°C.					25±3°C.
			satisfy the specifications in the following table.	Let sit for 24±2h at room condition*, then measure.					
	Appearance		No marking defects	The charge/discharge current is less than 50mA.					
		Capacitance Change	Within ±3.0% or ±0.3pF	7					
			(Whichever is larger)	J					
	Q		Q ≥ 350						
	i í	I.R.	More than 1,000M $\Omega$ or 50 M $\Omega$ · $\mu$ F	1					
			(Whichever is smaller)						
6	Extern	nal Visual	No defects or abnormalities	Vis	sual inspect	tion			
7	Phisic	al Dimension	Within the specified dimensions	Us	sing Measur	ring instrum	ent of dimens	ion.	
8	Resist	tance to	The measured and observed characteristics should	Im	merse the o	capacitor in	a solder solut	tion at 260±5	5°C
	Soldering Heat		satisfy the specifications in the following table.	for	r 10±1s Le	et sit at room	condition* fo	r 24±2h, the	n measure.
	1	Appearance	No marking defects	]					
		Capacitance	Within ±5% or ±0.5pF						
		Change	(Whichever is larger)						
	i í	Q	Q ≥ 1,000						
	1	I.R.	More than 10,000M $\Omega$ or 500 M $\Omega \cdot \mu F$	1					
			(Whichever is smaller)						
9	Solde	rability	95% of the terminations is to be soldered evenly and	Те	est Method	: Solder b	bath method		
			continuously.	Flu	ux	: Solutior	n of rosin etha	anol 25(mas	s)%
				Pre	eheat	: 80°C to	120°C for 10s	to 30s	
				So	older	: Sn-3.0A	g-0.5Cu		
				So	older Temp.	: 245+/-5	°C		
				Im	mersion tim	ne : 2+/-0.5	s		

\*Room Condition : Temperature:15°C to 35°C, Relative humidity:45% to 75%, Atmosphere pressure:86kPa to 106kPa

# Specification and Test Methods

No.	Test Item		Test Item Specification		Test Method				
10	Electrical	Apperance	No defects or abnormalities	Visu	al inspection.				
	Characte- rization	Capacitance Change	Within the specified tolerance	The and	capacitance/Q voltage shown	should be measured in the table.	d at 25°C at the fre	equency	
		Q	Q ≥ 1,000		Cap. tem	less than 1,000pF	1,000pF or more		
					Frequency	1±0.1MHz	1±0.1kHz		
				L	Voltage	0.5 to 5V(r.m.s.)	1±0.2V(r.m.s.)		
		I.R. 25 °C	More than 100,000M $\Omega$ or 1,000 M $\Omega$ ·µF (Whichever is smaller)	The DC5	insulation resis	tance should be mea °C and 125 °C with	asured with a iin 1 min. of charg	ing.	
		I.R. 125°C	More than 10,000MΩ or 100 MΩ·μF (Whichever is smaller)						
		Dielectric Strength	No failure	No f betw char	ailure should be veen the termina rge/discharge co Rated Voltag DC630V	e observed when vol ations for 1s to 5s, p urrent is less than 50 e Test Volta 150% of the rate	tage in Table is ap rovided the 0mA. ge	oplied	
11	Board	Appearance	No marking defects	Solo	ler the capacito	r on the test iig (glas	s epoxy board) sh	iown	
	Flex	Capacitance	Within ±5.0% or ±0.5pF	in Fi	ig1 using a sold	er. Then apply a for	ce in the		
		Change	(Whichever is larger)	dired by th the s	ction shown in F ne reflow metho soldering is unif	ig 2 for 5±1s. The s d and should be cor orm and free of defe	oldering should be iducted with care s ects such as heat s	e done so that shock.	
42	Terminol	Appeorance	fig.1 t : 1. 6mm		Type GCH21 C GCH31 2 GCH32 2 GCH32 2 GCH32 2 GCH32 2 Fig.:	a b 0.8 3.0 2.0 4.4 2.0 4.4 50 min. Pressurizing speed:1.0mm/s Pressurize Flexure (High D 2	C 1.3 1.7 2.6 (in mm) : 3 ielectric Type)		
12	Terminal Strength	Appearance Capacitance	No marking defects Within specified tolerance	Solc in Fi	ler the capacito	r to the test jig (glass ler. Then apply 18N	s epoxy board) she force in parallel	own	
		Change		with	the test jig for 6	60s.			
		Q	Q ≥ 1,000	The	soldering shoul	d be done by the ref	low method and s	hould	
		I.R.	More than 10,000M $\Omega$ or 500 M $\Omega$ · $\mu$ F (Whichever is smaller)	be c of de	onducted with one of the conducted with one of the conducted with a second con	are so that the sold	ering is uniform ar	nd free	
					Type   GCH21 1   GCH31 2   GCH32 2	a b .2 4.0 1 2.2 5.0 2 2.2 5.0 2	C .65 2.0 2.9 (in mm)		
						→ 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	c c c c c c c c c c c c c c	mm)	

## Specification and Test Methods

No.	Test Item		Specification	Test Method
13	Beam Load Te	est	Destruction value should be exceed following one. < Chip L dimension : 2.5mm max. > Chip thickness > 0.5mm rank : 20N Chip thickness ≤ 0.5mm rank : 8N < Chip L dimension : 3.2mm min. > Chip thickness < 1.25mm rank : 15N Chip thickness ≥ 1.25mm rank : 54.5N	Place the capacitor in the beam load fixture as Fig 4. Apply a force. < Chip L dimension : 2.5mm max. > Iron Board < Chip L dimension : 3.2mm min. > Iron Board Fig.4 Speed supplied the Stress Load : 2.5mm / s
14	Capacitance Temperature Characteris- tics	Capacitance Change Capacitance Drift	0±30 ppm/°C (Temp.Range:+25 to +125°C) 0+30,-72 ppm/°C (Temp.Range:-55 to +25°C) Within ±0.2% or ±0.05 pF (Whichever is larger.)	The capacitance change should be measured after 5min. at each specified temperature stage.The temperature coefficient is determind using the capacitance measured in step 3 as a reference.When cycling the temperature sequentially from step1 through 5 the capacitance should be within the specified tolerance for the temperature coefficient.The capacitance drift is caluculated by dividing the differences between the maximum and minimum measured values in the step 1,3 and 5 by the capacitance value in step 3.StepTemperature(°C)1 $25\pm 2$ 2 $-55\pm 3$ 3 $25\pm 2$ 4 $125\pm 3$ 5 $25\pm 2$

Package

#### (1) Appearance of taping

(a) Paper Tape

Bottom Tape (Thickness: Around  $50\mu m$ ) is attached below Base Tape with sprocket and put Top Tape (Thickness: Around  $50\mu m$ ) on capacitor.

(b) Plastic Tape

Cover Tape (Thickness: Around 60µm) is put on capacitor on Base Tape (Blister carrier Tape).

- (c) The sprocket holes are to the right as the Tape is pulled toward the user.
- (2) Packed chips



#### (3) Dimensions of Tape

(a) Type A (Dimensions of chip : Apply to 1.6x0.8 , 2.0x1.25 , 3.2x1.6 , 3.2x2.5)



(Unit : mm)

	Dimensions of chip [L×W]	A*	B*	
ĺ	1.6×0.8	1.05	1.85	
ĺ	2.0×1.25	1.45	2.25	
ĺ	3.2×1.6	2.0	3.6	
	3.2×2.5	2.9	3.6	*Dimensions of A,B : Nominal value

(b) Type B (Dimensions of chip : Apply to 4.5x2.0)



Package

(c) Type C (Dimensions of chip : Apply to 4.5x3.2 to 5.7x5.0)



(5) Part of the leader and part of the empty tape shall be attached to the end of the tape as follows.



(Unit : mm)

(6) The top tape or cover tape and base tape are not attached at the end of the tape for a minimum of 5 pitches.

- (7) Missing capacitors number within 0.1% of the number per reel or 1pc, whichever is greater, and not continuous.
- (8) The top tape or cover tape and bottom tape shall not protrude beyond the edges of the tape and shall not cover sprocket holes.
- (9) Cumulative tolerance of sprocket holes, 10 pitches : ±0.3mm.

(10) Peeling off force : 0.1 to 0.6N in the direction shown on the follows.

